

FIG. 1
(PRIOR ART)

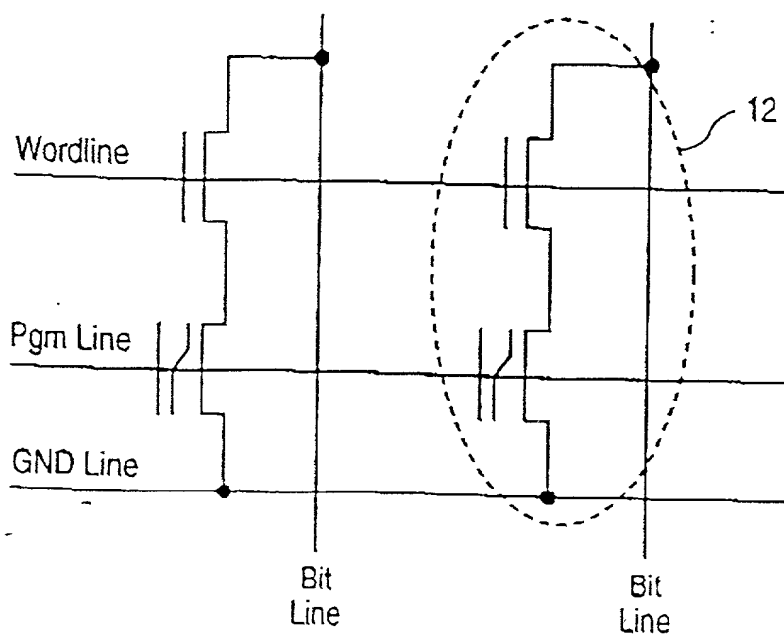


FIG. 2
(PRIOR ART)

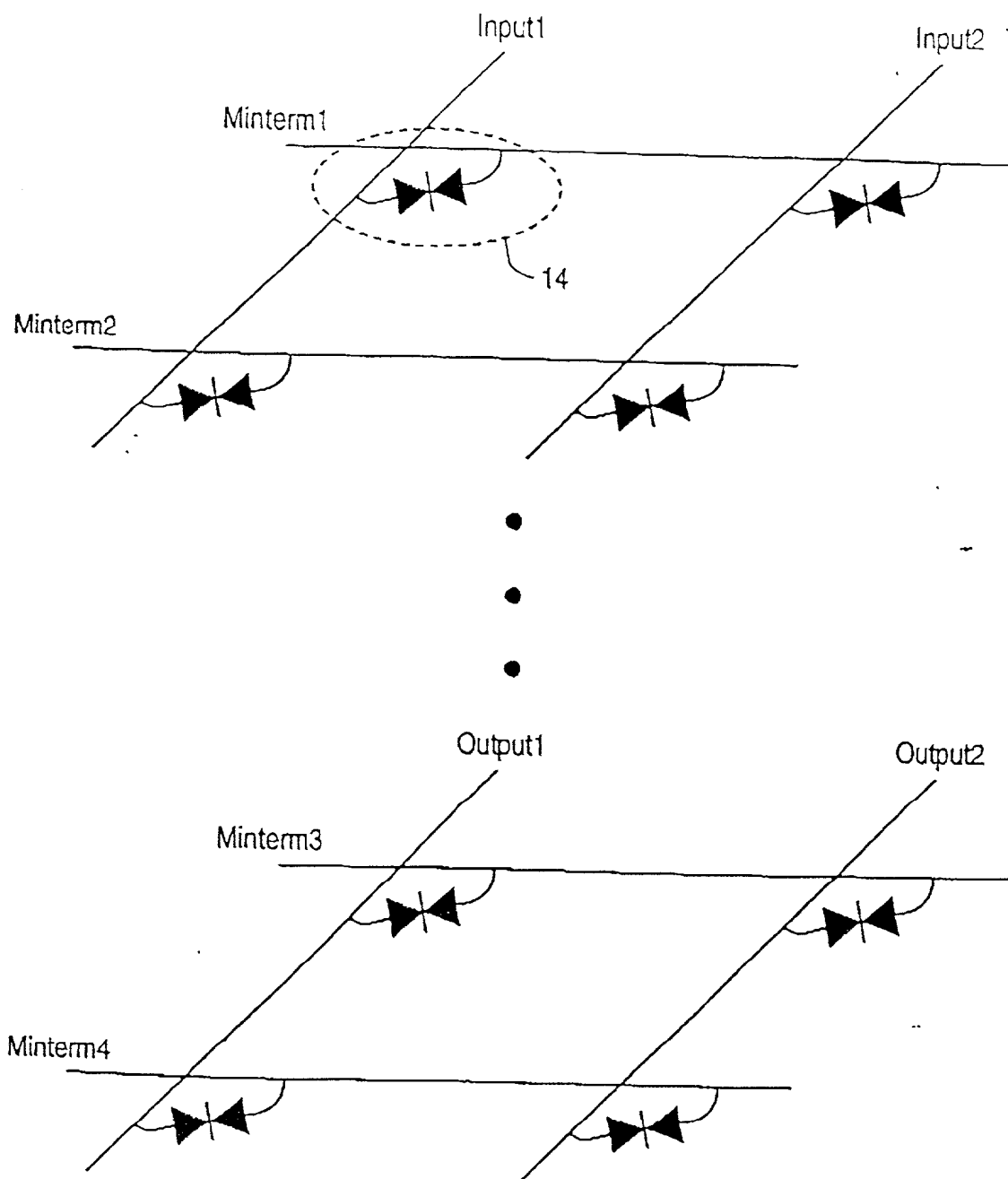


FIG. 3
(PRIOR ART)

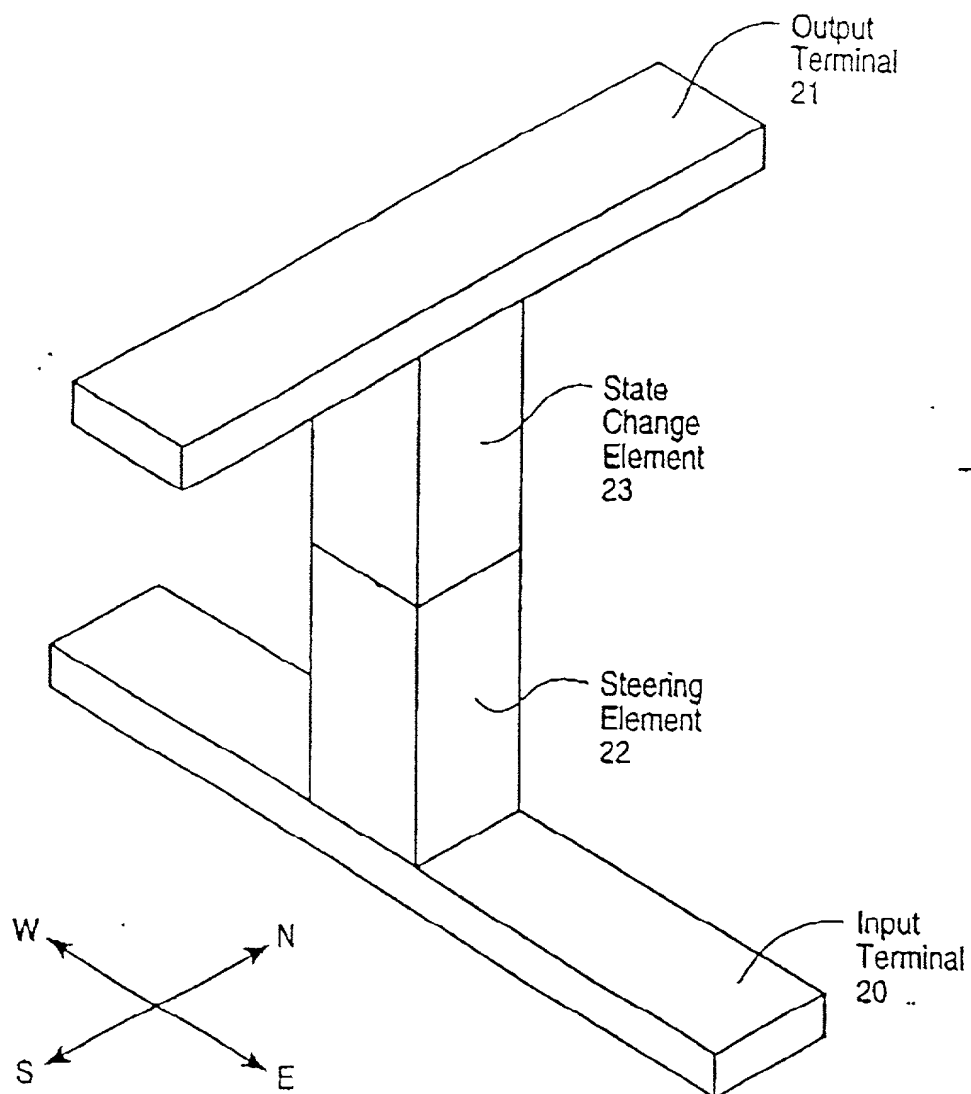


FIG. 4(a)

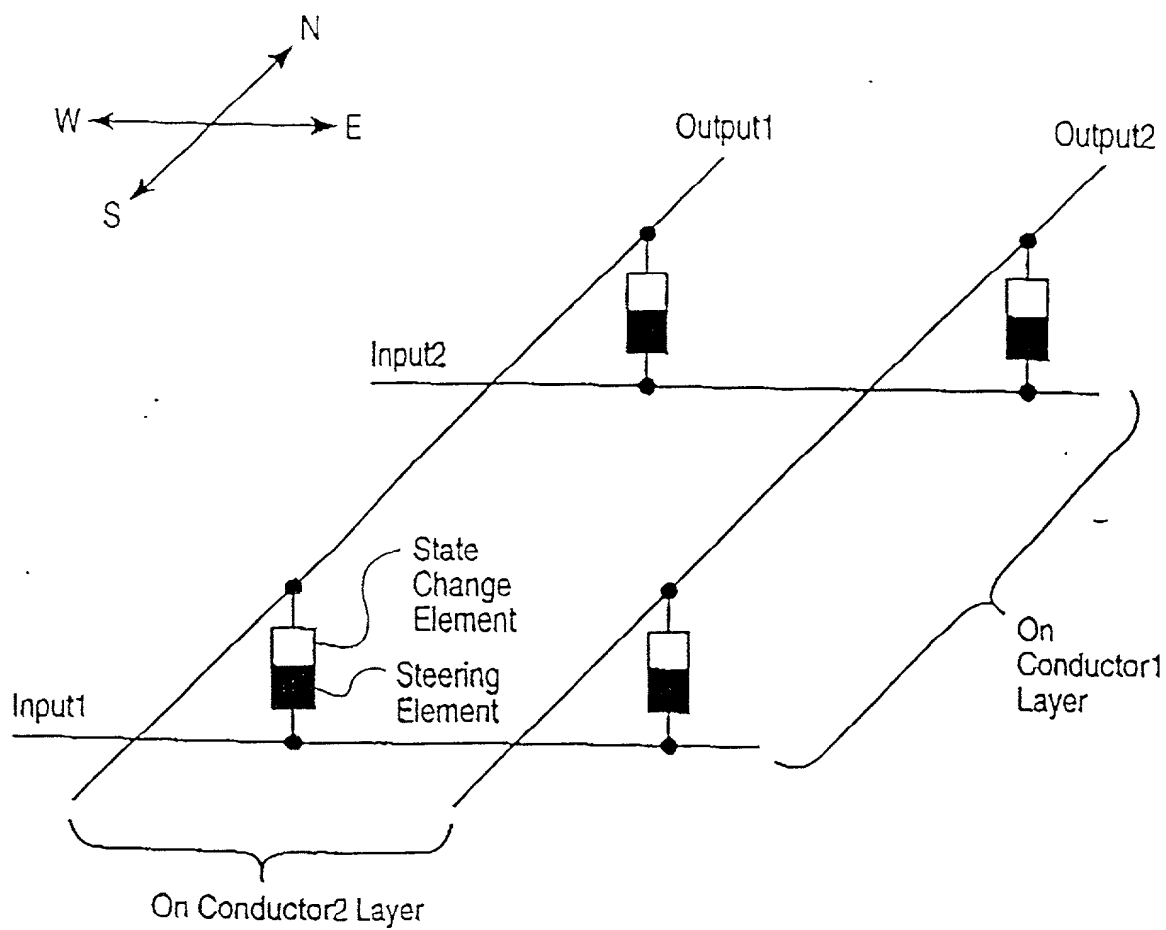


FIG. 4(b)

This diagram shows a cross-sectional view of a semiconductor device. It features a stack of seven horizontal conductive layers, labeled Conductor1 through Conductor7 from bottom to top. Between these conductive layers are six vertical pillars, labeled Pillar1 through Pillar6 from bottom to top. The pillars are formed by a core material (labeled 27) surrounded by a cladding material (labeled 26). The conductive layers are separated by insulating spacers (labeled 29). The entire structure is supported by a substrate (labeled 25). The conductive layers are shown with diagonal hatching, and the pillars are shown with a central core and an outer cladding.

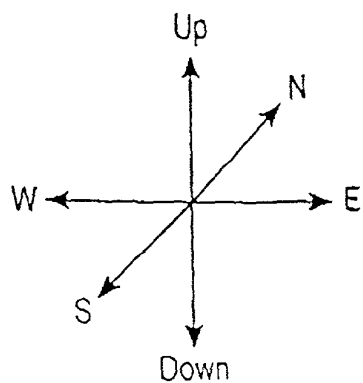


FIG. 5

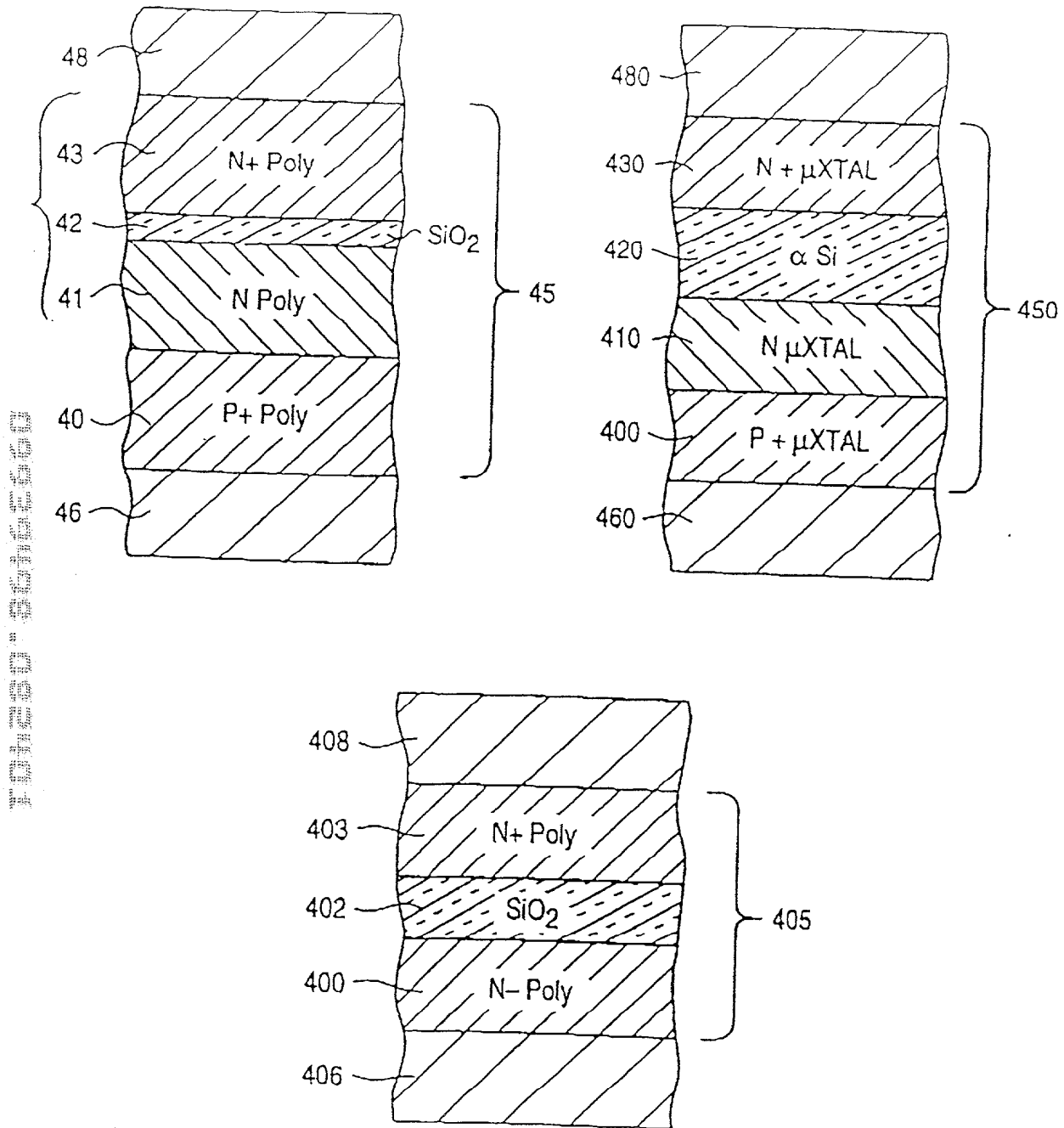


FIG. 6(a)

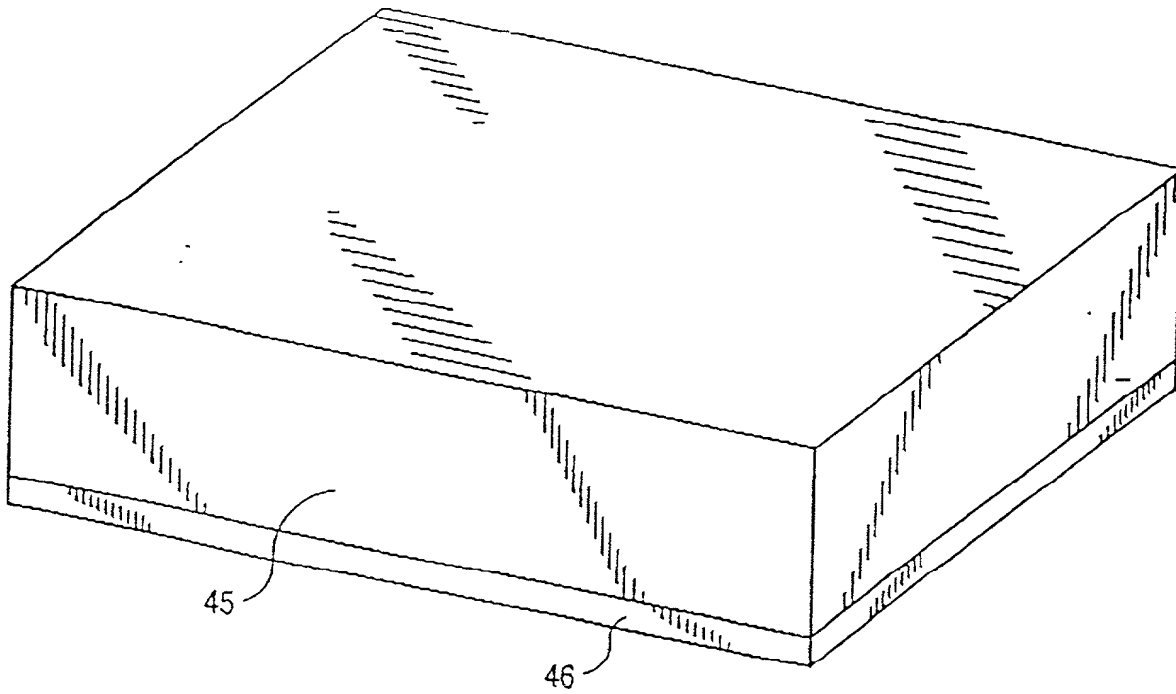


FIG. 6(b)

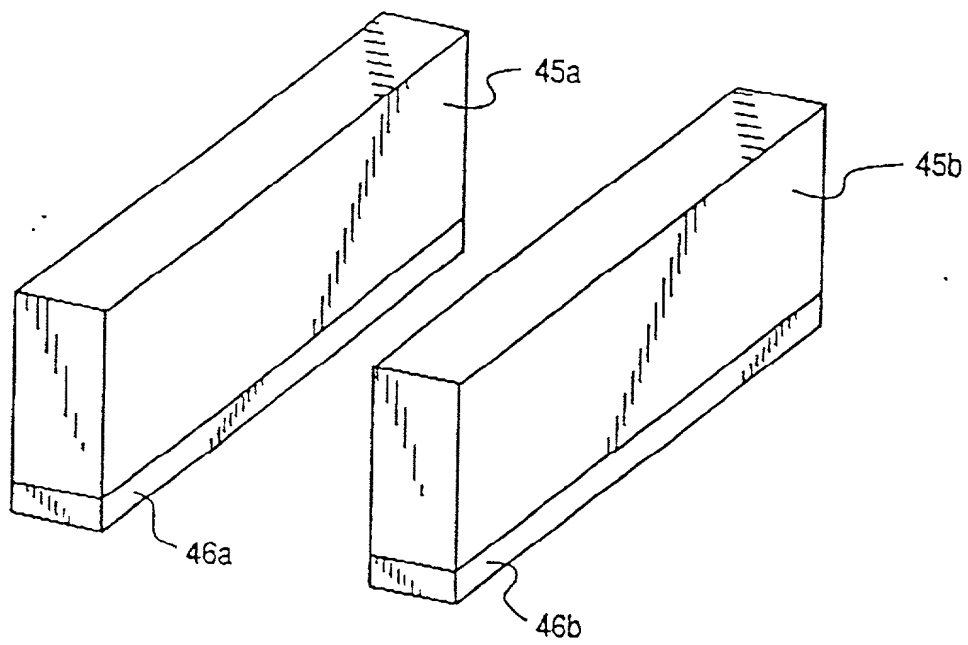


FIG. 6(c)

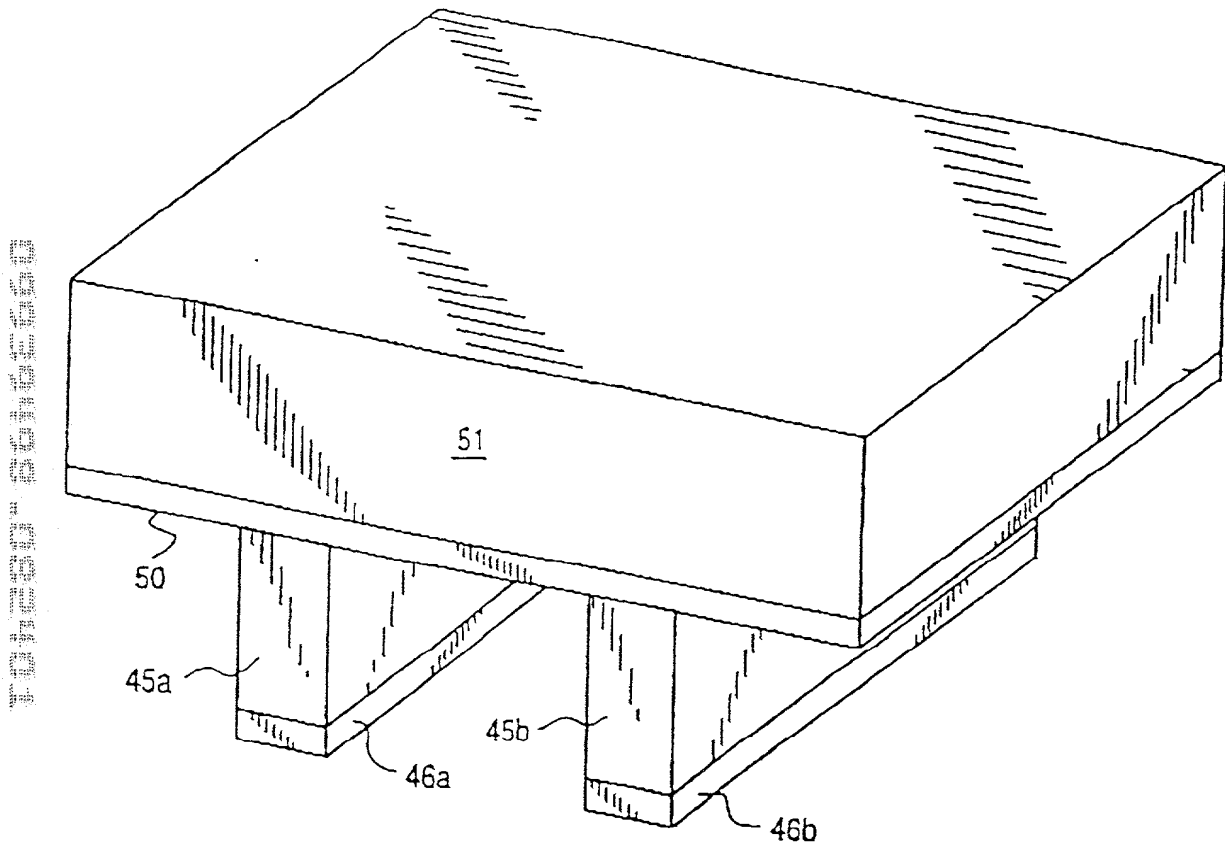


FIG. 6(d)

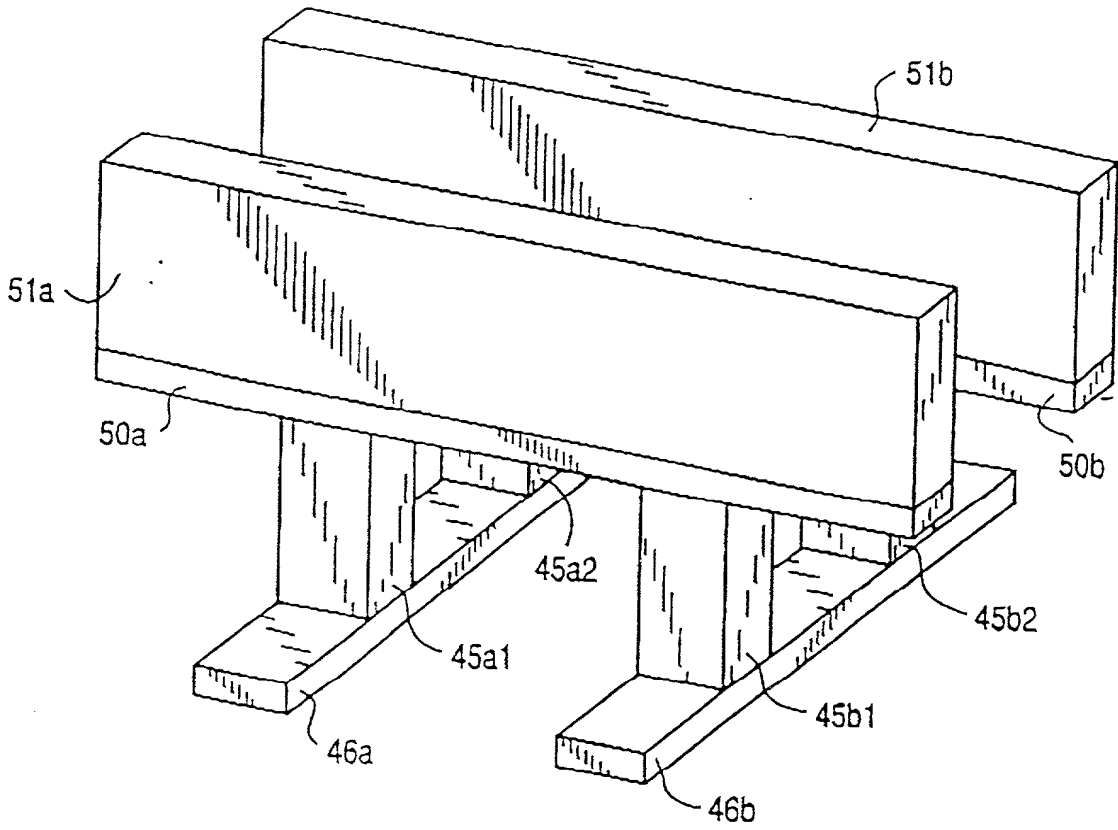


FIG. 6(e)

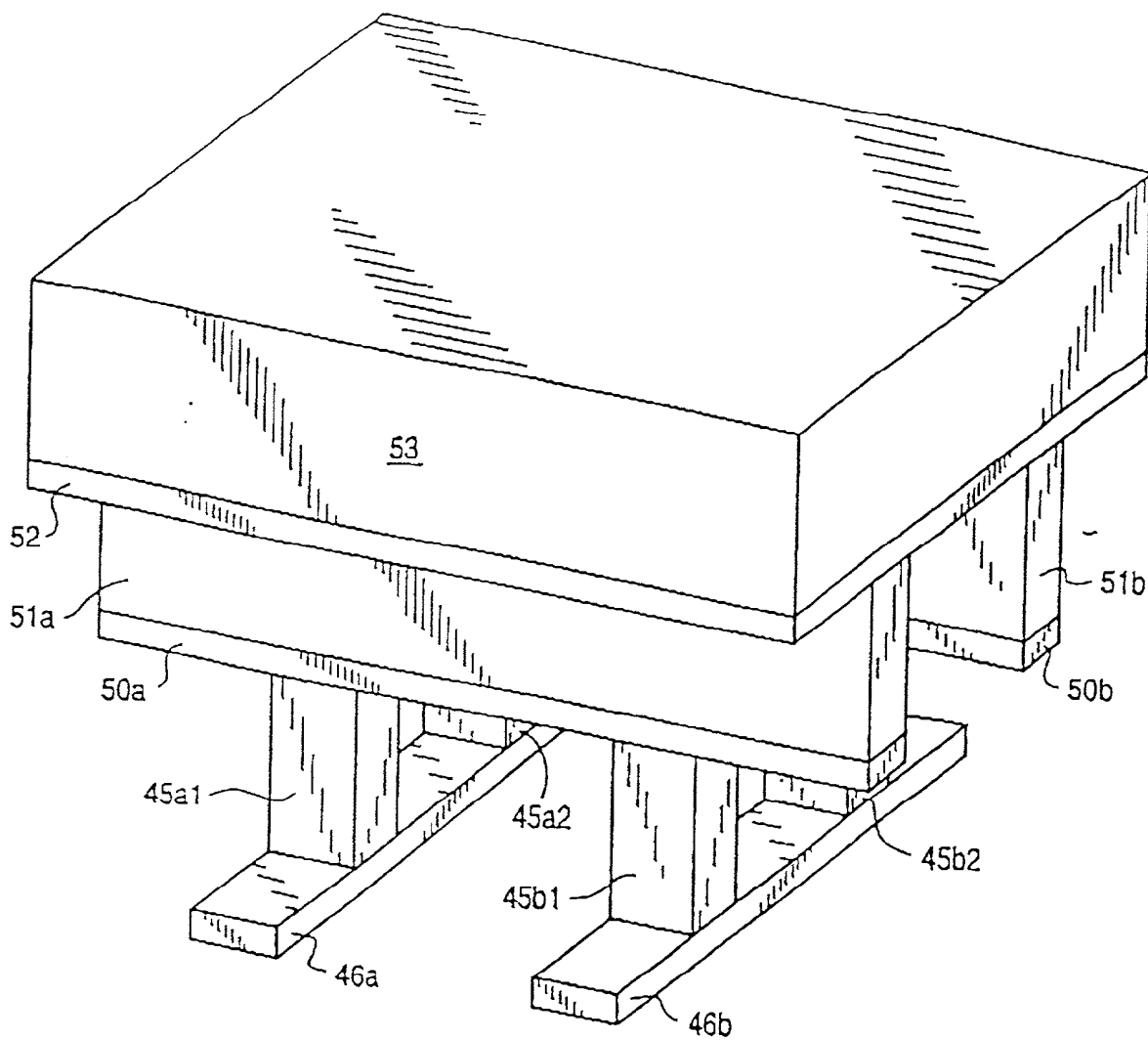


FIG. 6(f)

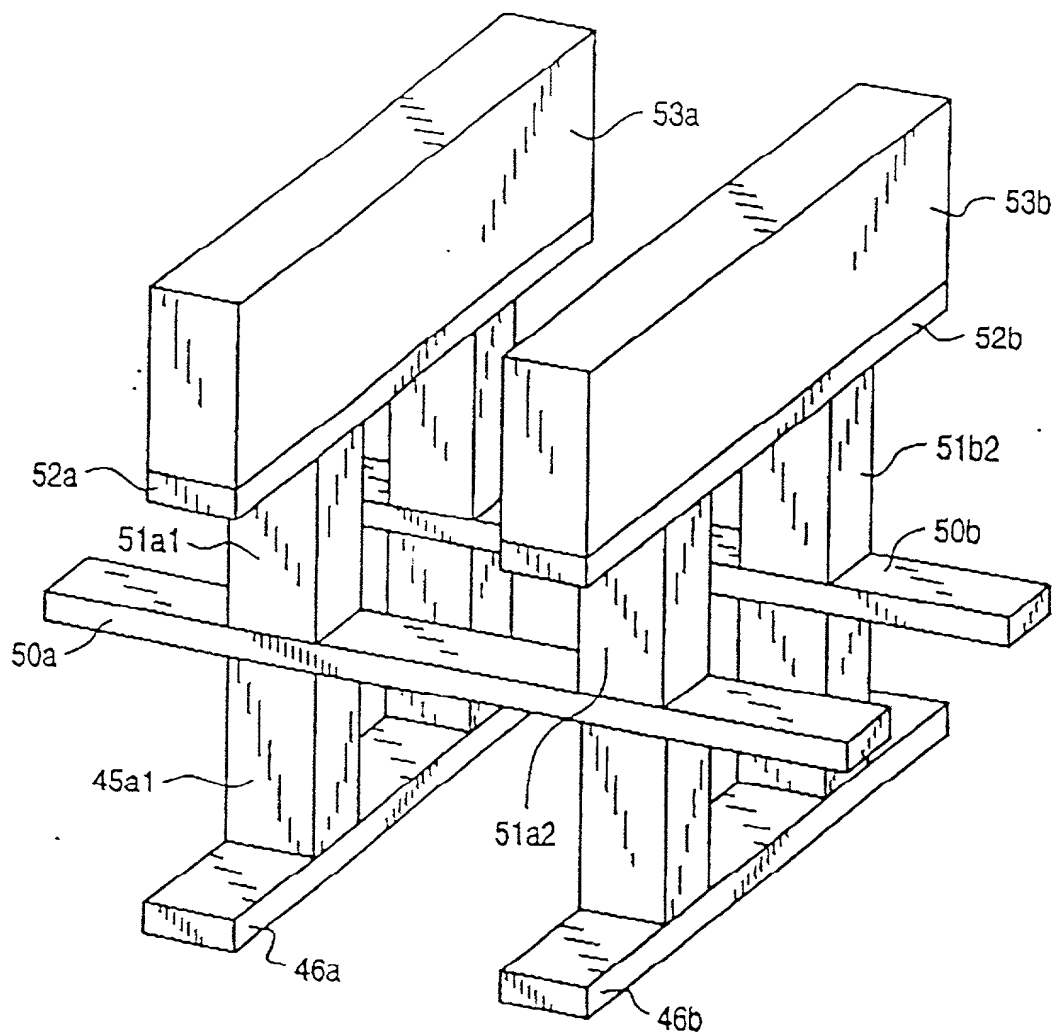


FIG. 6(g)

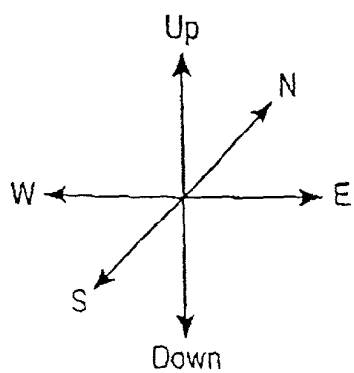


FIG. 7

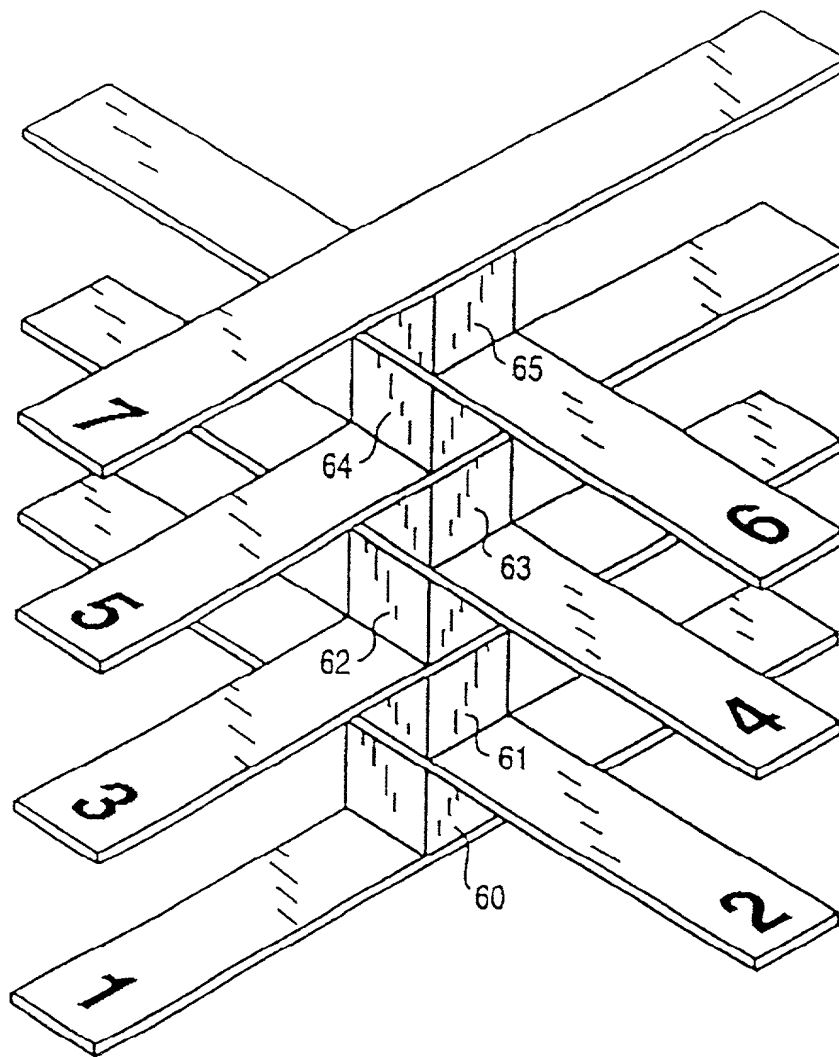


FIG. 8(a)

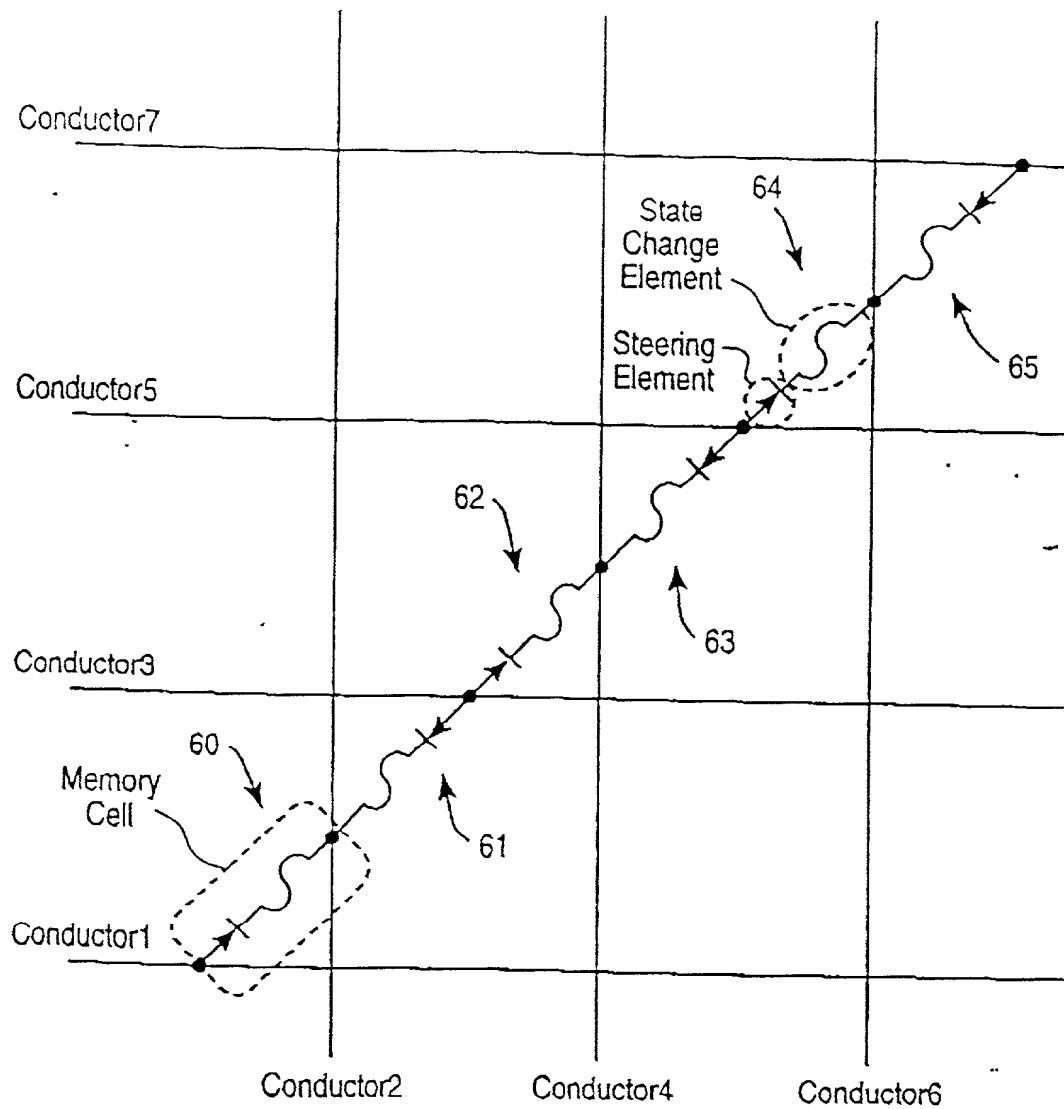


FIG. 8(b)

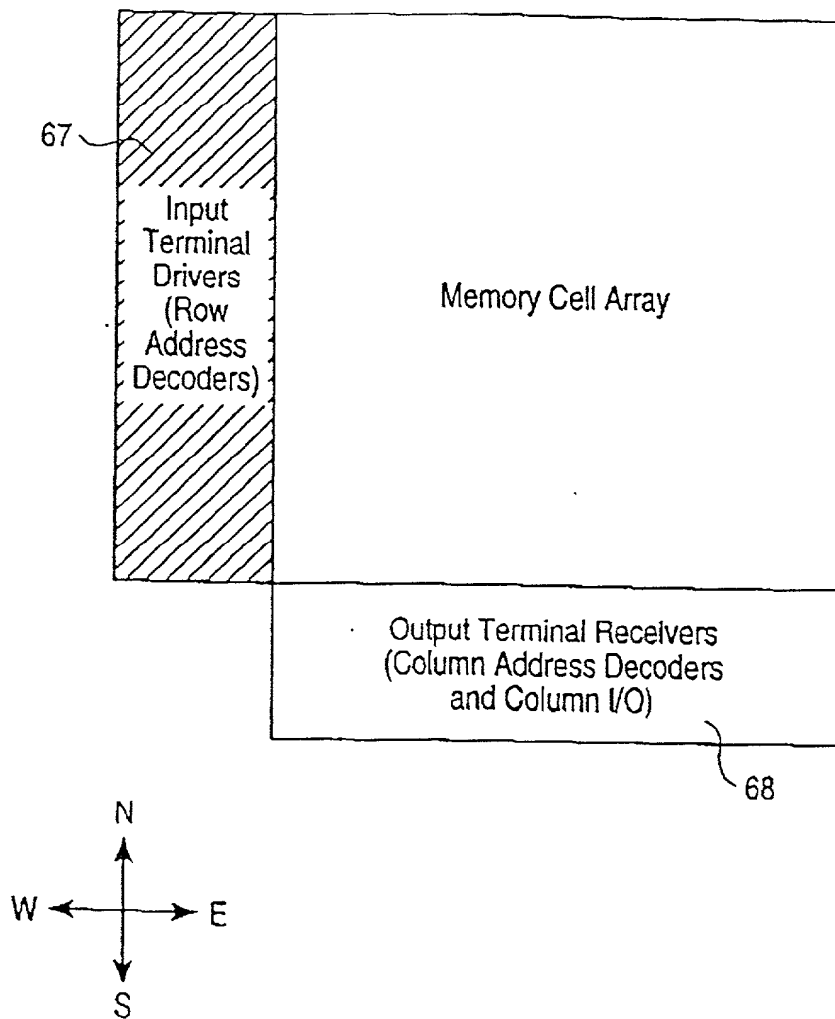


FIG. 9(a)

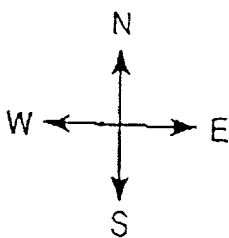
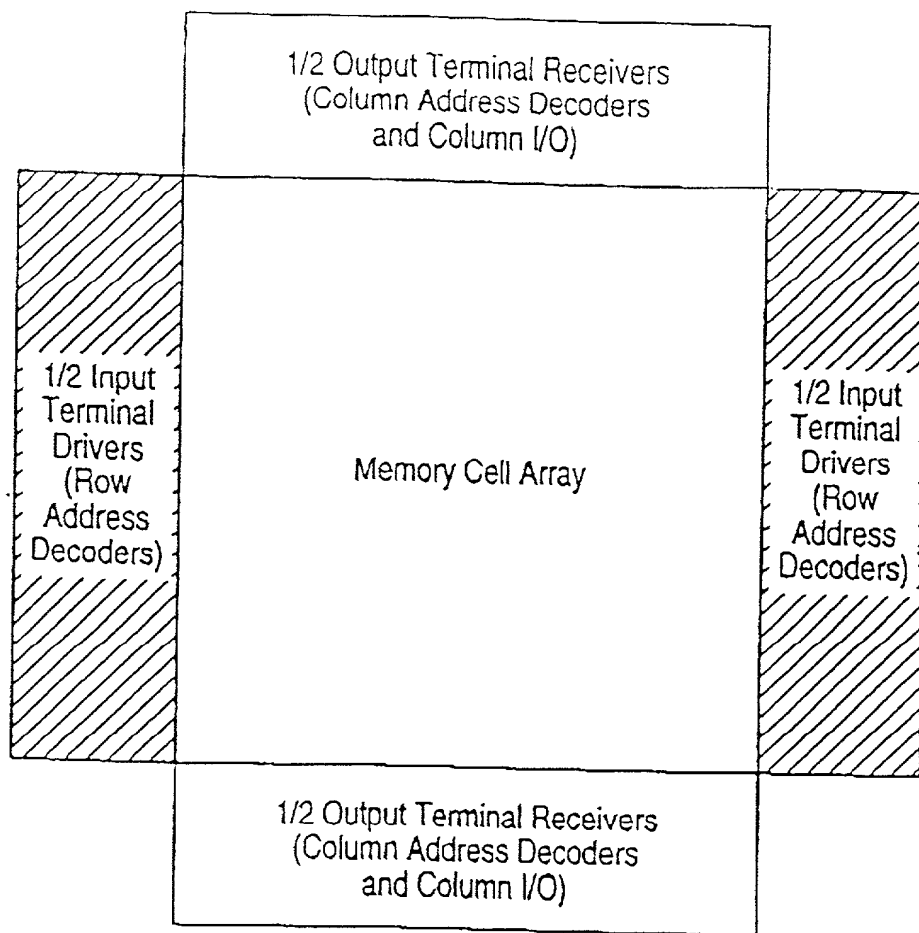


FIG. 9(b)

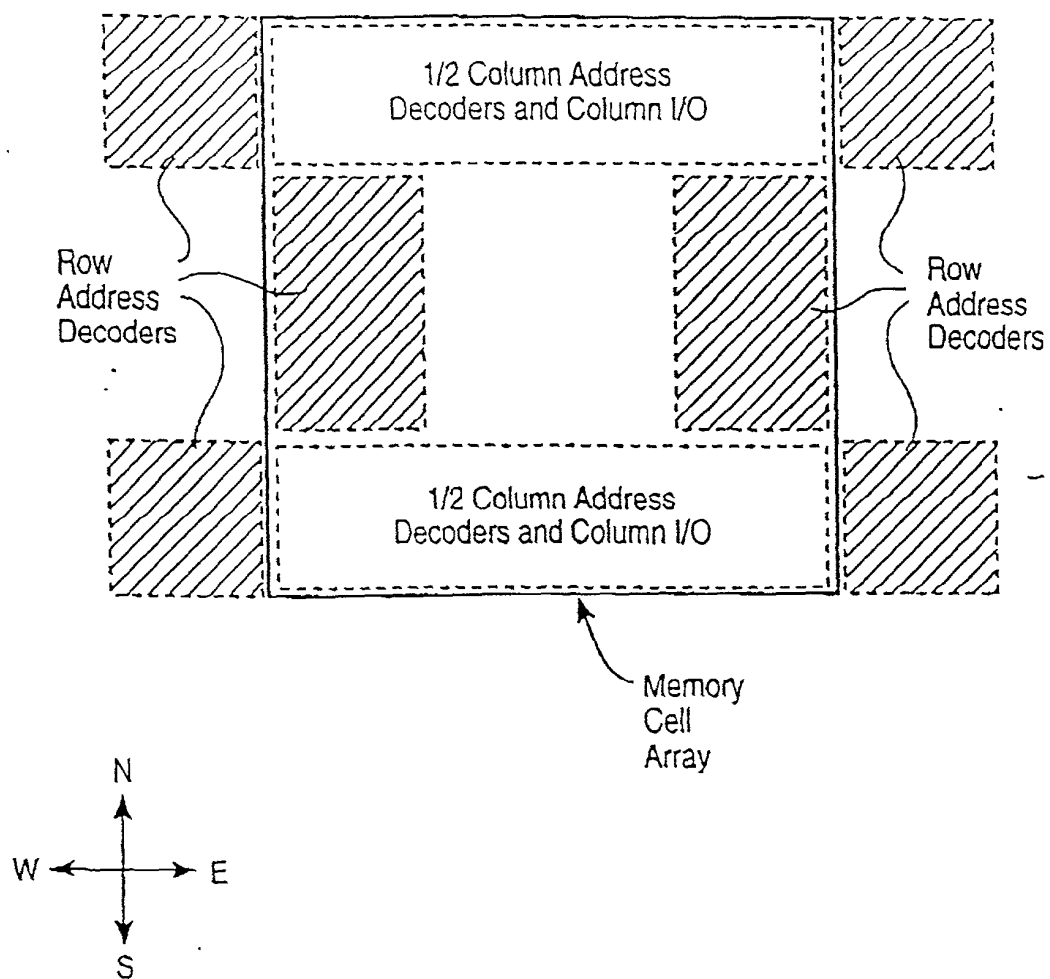
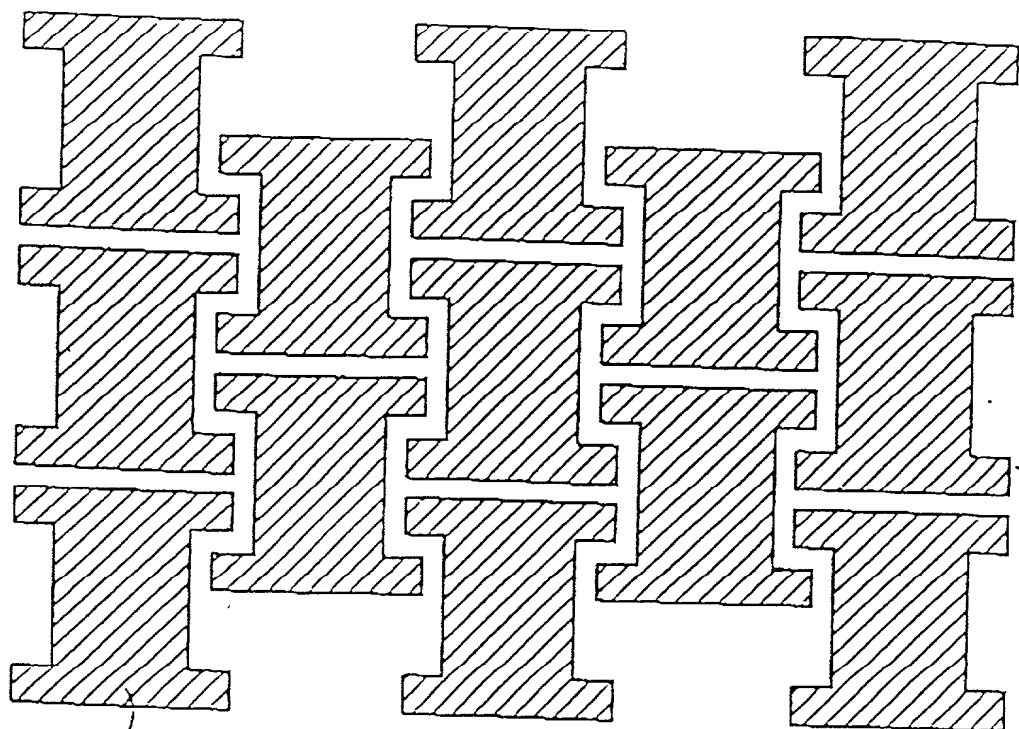


FIG. 9(c)



One Subarray

FIG. 9(d)

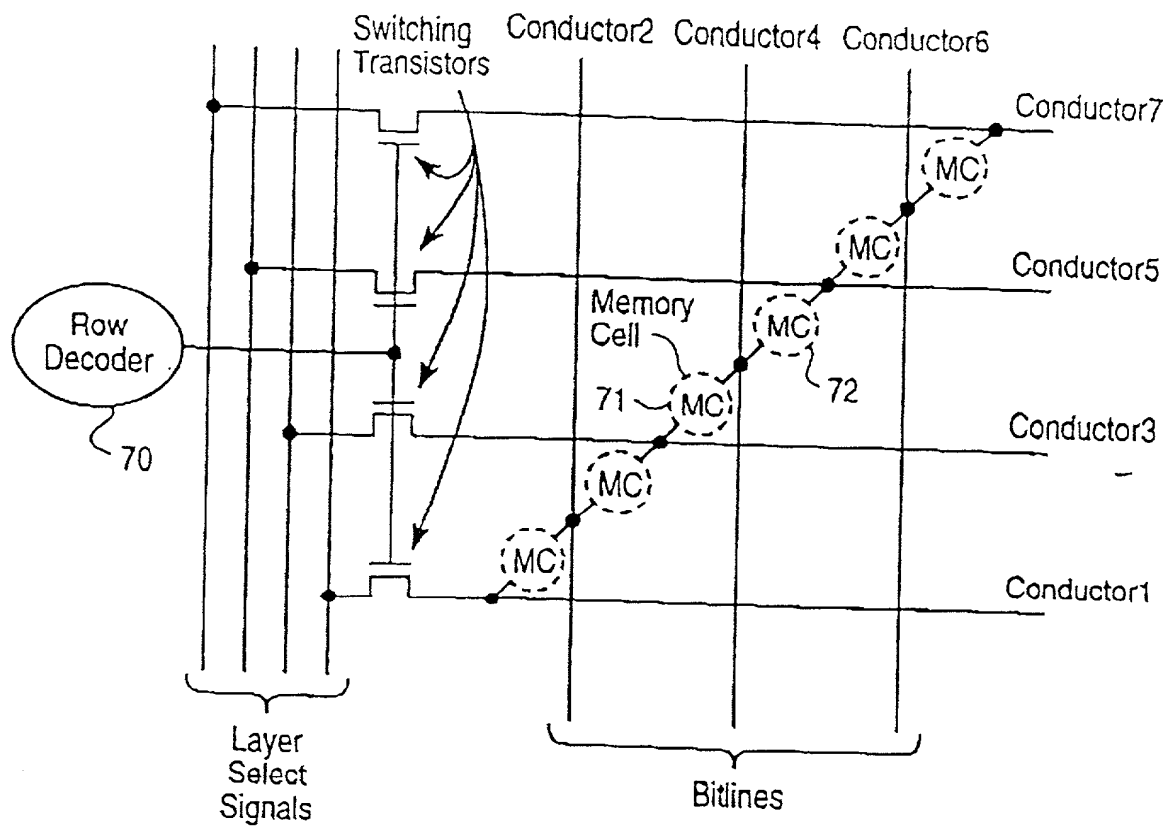


FIG. 10(a)

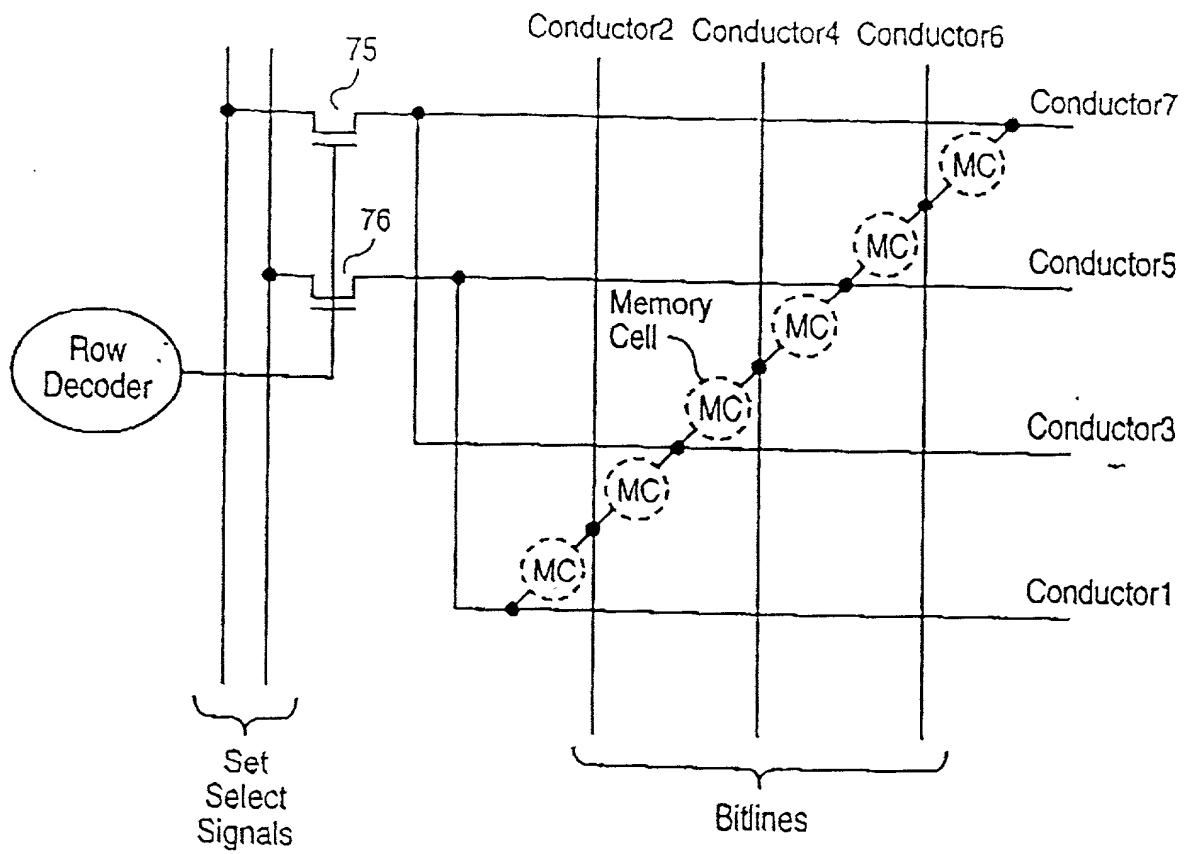


FIG. 10(b)

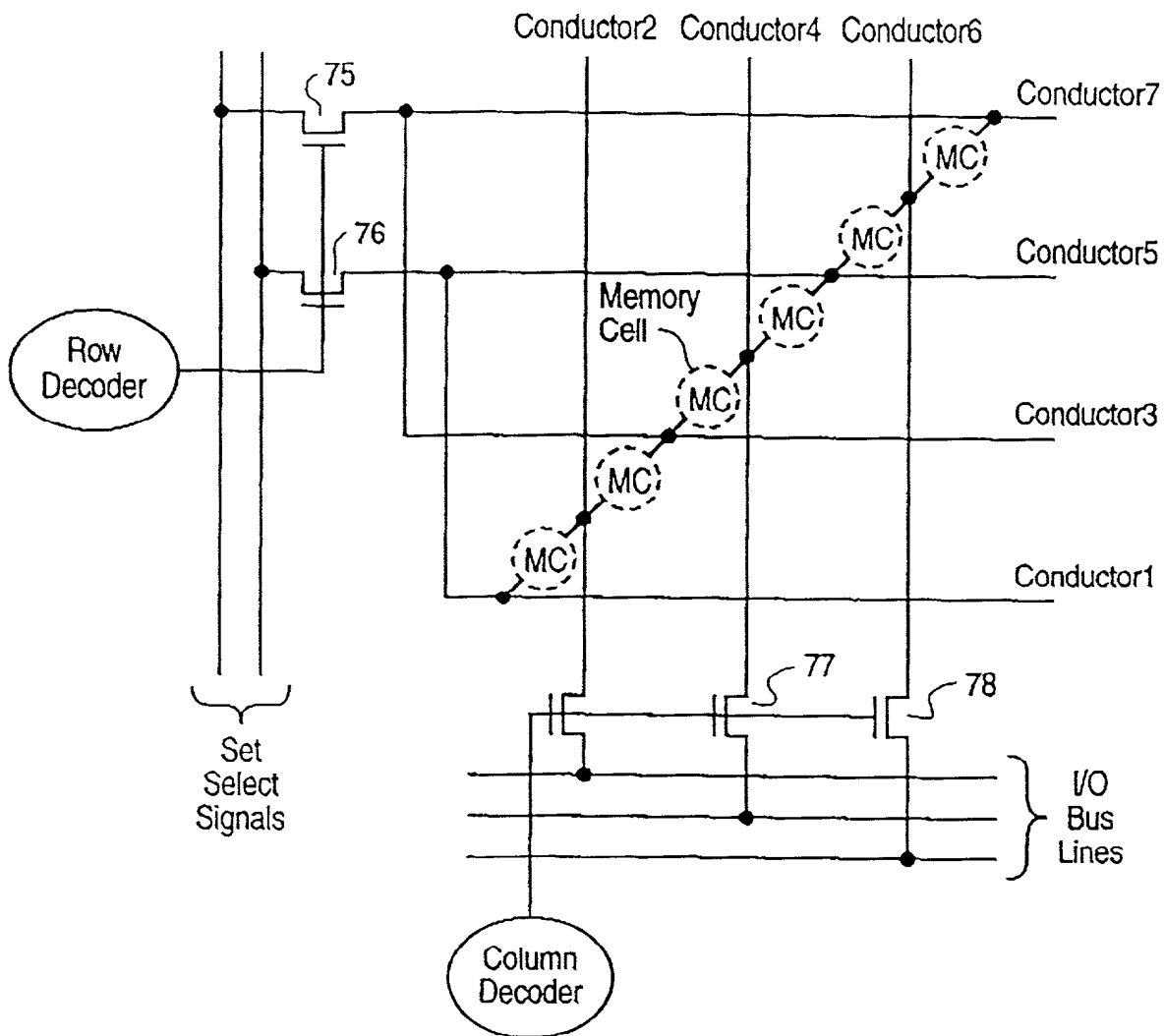


FIG. 11

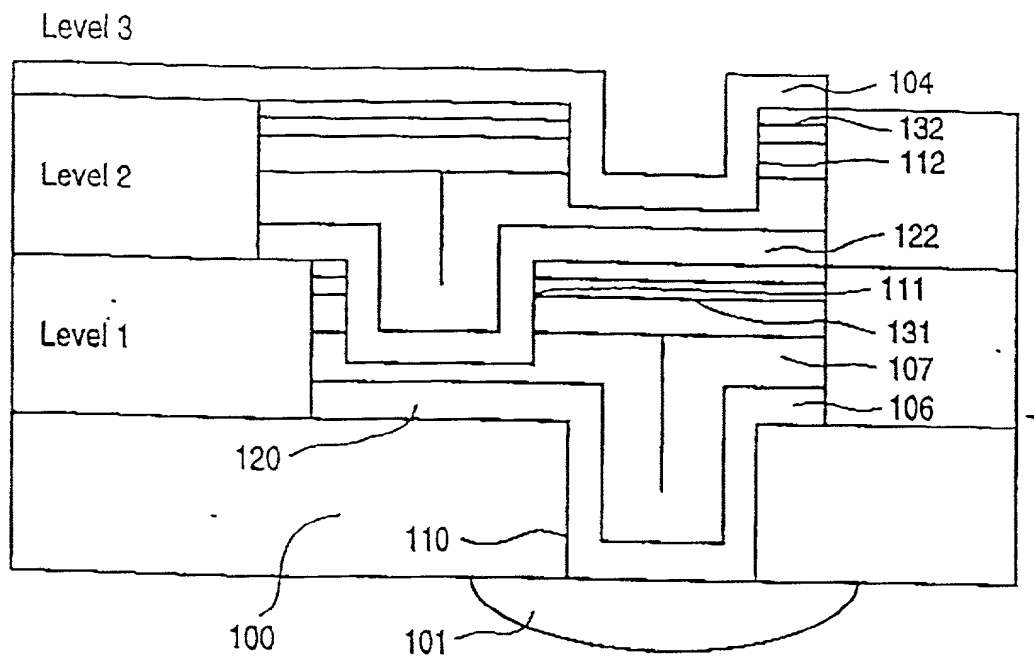


FIG. 12

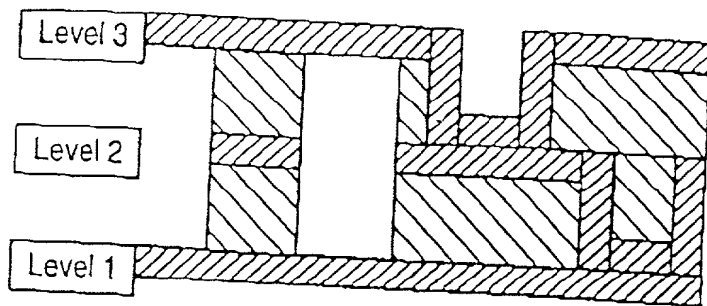


FIG. 13(a)

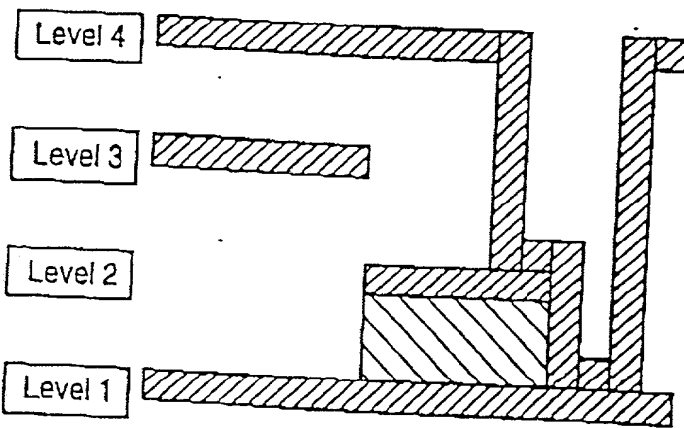


FIG. 13(b)

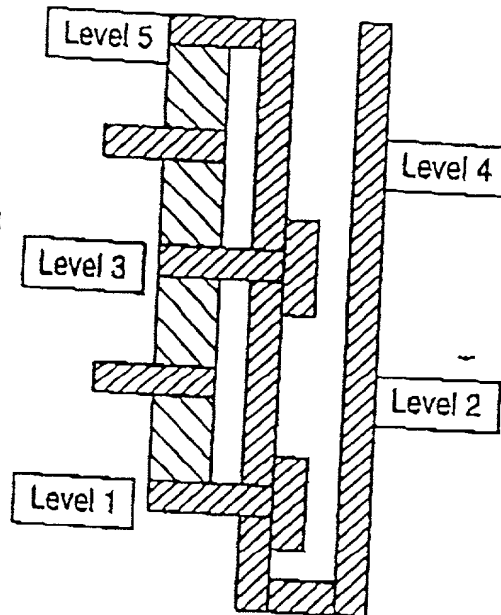


FIG. 13(c)

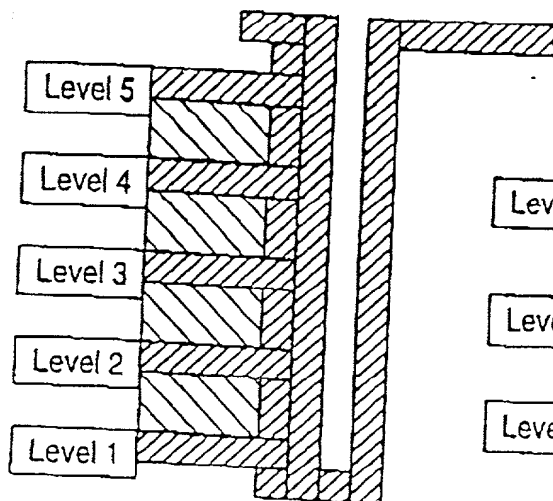


FIG. 13(d)

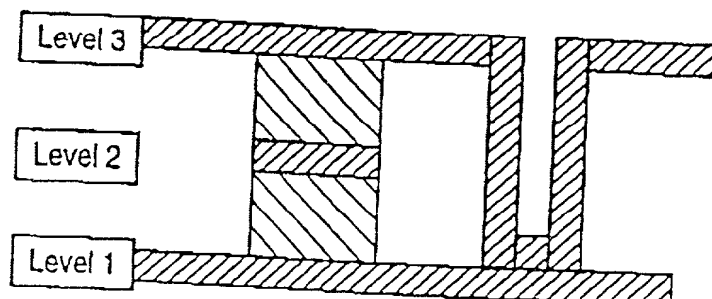


FIG. 13(e)